Amendments to the Claims:

Please amend the claims as follows:

1. (Currently Amended) An information processing apparatus comprising:

a data storing device;

first and second data input/output devices giving access to the data storing device;

a clock generating device comprising a clock oscillating section generating a normal clock signal to be supplied to ~~the first and~~ the second data input/output ~~devices~~ device, and a clock wait control section generating a wait clock signal having a cycle which is integer times as much as the normal clock signal has;

a control signal selector switching access of the first data input/output device or the second data input/output device to the data storing device; and

an access arranging device causing the clock oscillating section to stop the normal clock signal to the second data input/output device for one clock cycle, causing the clock wait control section to supply the wait clock signal to the second data input/output device, not allowing the second data input/output device to access the data storing device for one clock cycle, executing the access of the first data input/output device for the one clock cycle when a contention of the access of the first data input/output device and the second data input/output device to the data storing device is generated, and starting the access of the second data input/output device after the access of the first data input/output device for the one clock cycle is ended.

2. (Previously Presented) An information processing apparatus comprising:

a built-in memory;

a processor for processing data stored in the built-in memory;

a clock generating device comprising a clock oscillating section generating a normal clock signal to be supplied to the processor, and a clock wait control section generating a wait clock signal having a cycle which is integer times as much as the normal clock signal has;

an input/output control device executing access to the built-in memory upon receipt of an instruction from an external control device; and

an access arranging device causing the clock oscillating section to stop the normal clock signal for one clock cycle, causing the clock wait control section to supply the wait clock signal to the processor, and carrying out access of the input/output control device with a priority when a contention of access of the processor and the input/output control device to the built-in memory is generated.

3. (Previously Presented) The information processing apparatus according to claim 2, further comprising a selecting device switching the access of the processor and the input/output control device to the built-in memory,

wherein the access arranging device outputs a control signal to the selecting device when a request for the access of the input/output control device to the built-in memory is generated during the access of the processor to the built-in memory, and

the selecting device receiving the control signal switches the access of the processor to the access of the input/output control device to the built-in memory.

4. (Previously Presented) The information processing apparatus according to claim 2, further comprising a holding device for holding read data output from the built-in memory before a wait operation of the processor during the wait operation of the processor,

wherein the access arranging device switches read data to be supplied to the processor between the read data output from the built-in memory and the read data held by the holding device.

5. (Currently Amended) A memory access arranging method of an information processing apparatus including data storing device, first and second data input/output devices giving access to the data storing device, and a clock generating device comprising a clock oscillating section generating a normal clock signal for supplying to ~~the first and~~ the second data input/output ~~devices~~ device and a clock wait control section generating a wait clock signal having a cycle which is integer times as much as the normal clock signal has, the method comprising the steps of:

providing the normal clock signal to the first and second data input/output devices;

providing the clock wait signal to cause the normal clock signal for the second data input/output device to be stopped for one clock cycle and not allowing the second data input/output device to access the data storing device for one clock cycle when a contention of the access of the first data input/output device and the second data input/output device to the data storing device is generated;

executing the access of the first data input/output device earlier than the second data input/output device; and

canceling the stop of the clock signal of the second data input/output device after ending the access of the first data input/output device, and executing the access of the second data input/output device.

6. (Previously Presented) A memory access arranging method of an information processing apparatus including a processor for carrying out a pipeline processing over an instruction, a memory provided in the processor, and an input/output control device executing access to the memory with a higher priority than the processor, and a clock generating device comprising a clock oscillating section generating a normal clock signal for supplying to the processor and the data input/output device, and a clock wait control section generating a wait clock signal having a cycle which is integer times as much as the normal clock signal has, the method comprising the steps of:

providing the normal clock signal to the processor and the data input/output device;

generating a wait request signal for causing a clock signal supplied to the processor to be stopped for one clock cycle when a contention of access of the processor and the input/output control device to the memory is generated;

providing the clock wait signal to cause the normal clock signal for the processor to be stopped for one clock cycle and not allowing the processor to access the memory for one clock cycle when a contention of the access of the data input/output device and the processor to the memory is generated;

switching the access of the processor to the access of the input/output control device to the memory; and

canceling the wait request signal after ending the access of the input/output control device to the memory, and executing the access of the processor to the memory.

7. (Previously Presented) A memory access arranging method of an information processing apparatus having a processor for carrying out a pipeline processing over an instruction, a memory provided in the processor, an input/output control device for executing

access to the memory with a higher priority than the processor, a clock generating device comprising a clock oscillating section generating a normal clock signal for supplying to the processor and the data input/output device, and a clock wait control section generating a wait clock signal having a cycle which is integer times as much as the normal clock signal has, and a holding device for holding read data output from the memory before a wait operation of the processor during the wait operation of the processor, comprising the steps of:

providing the normal clock signal to the processor and the data input/output device;

holding the read data output from the memory before the wait operation of the processor when a contention of read access of the input/output control device is generated for a period in which the processor gives continuous read access to the memory;

providing the clock wait signal to cause the normal clock signal for the processor to be stopped;

executing the access of the input/output control device to the memory; and

canceling the stop of the clock signal of the processor after ending the access of the input/output control device to the memory, supplying the data held in the holding device to the processor, and restarting the access of the processor to the memory.